

# USB Type-C ENGINEERING CHANGE NOTICE

**Title: USB Type-C R2.4 LRD Cleanup ECR r2**

**Applied to: USB Type-C Specification Release 2.4, Oct 2024**

<b>Brief description of the functional changes proposed:</b>
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Items below relate to each proposed change:

A. Edit 6.1.2.4.1 to allow USB3.2 Active cables with just re-drivers.

B. Define when the USB3 U3 power is measured

C. Add reference for LRD cables to USB3.2 active cable section

D. Add TBD for USB4 gen4 retimed active cables. Updated USB4 gen2/3 retimed cable burst error measurement

E, H. Update LRD overview for USB4 gen4

F, K. Remove LRD Tuning register as not used in any cables and removed from USB4 Specification

G. Clarify the SB transactions are needed for TBT3, USB4 gen2/3, and USB4 gen4 for LRD active cables

I, J. Clarify USB4 gen4 ELT\_Recovery transitions to Forwarding on all lanes

<b>Benefits as a result of the proposed changes:</b>
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Match the current active cable ecosystem. Fix errors in the specification. Add USB4 gen4 requirements for retimed active cables.

<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
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None

<b>An analysis of the hardware implications:</b>
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None

<b>An analysis of the software implications:</b>
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None

<b>An analysis of the compliance testing implications:</b>
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USB-C Functional Test Specification will need to be updated.

# USB Type-C ENGINEERING CHANGE NOTICE

## Actual Change Requested

### (a). Section 6.1.2.4.1, Page 279

#### From Text:

##### 6.1.2.4.1 USB 3.2 Active Cable Architectures

Active cables may have the combinations of re-timers and re-drivers as illustrated in Figure 6-1. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope. Active cables shall support the features defined in Table 6-2.

#### To Text:

##### 6.1.2.4.1 USB 3.2 Active Cable Architectures

Active cables may have **different** the combinations of re-timers and re-drivers. **Some active cable examples are as** illustrated in Figure 6-1. **Other design options are possible. ~~Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope.~~** Active cables shall support the features defined in Table 6-2.

# USB Type-C ENGINEERING CHANGE NOTICE

## Actual Change Requested

(b). Table 6-6, Page 281

### From Text:

State	Maximum V <sub>CONN</sub> Power Consumption	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U1 power	Forwarding LFPS is required
U3	20 mW	Steady state power. eMarker in sleep.
Rx.Detect	20 mW	Rx.Detect period <i>may</i> be lengthened when no <b>USB 3.2</b> terminations have been detected. eMarker in sleep.
eSS.Disabled	20 mW	<b>USB 3.2</b> is disabled. eMarker in sleep.

### To Text:

State	Maximum V <sub>CONN</sub> Power Consumption	Power Consumption Notes
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U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U1 power	Forwarding LFPS is required
U3	20 mW	Steady state power. eMarker in sleep. <sup>1</sup>
Rx.Detect	20 mW	Rx.Detect period <i>may</i> be lengthened when no <b>USB 3.2</b> terminations have been detected. eMarker in sleep. <sup>1</sup>
eSS.Disabled	20 mW	<b>USB 3.2</b> is disabled. eMarker in sleep. <sup>1</sup>

1. Measured at ~~after the maximum least-tRaWeaken time~~ after Vconn is applied with no USB PD traffic for at least 500ms.

# USB Type-C ENGINEERING CHANGE NOTICE

## (c). 6.1.2.4.6 USB 3.2 Signal Swing, Page 281

### From Text:

#### 6.1.2.4.6 USB 3.2 Signal Swing

An active cable transmitter only must drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for USB 3.2 Gen2, if the transmitter is located in the cable plug next to the receiving port.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for USB 3.2 Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason. Figure 6-2 defines the SuperSpeed electrical test points and is copied from the **USB 3.2** specification. Figure 6-3 indicates the test points and test equipment connections.

### To Text:

#### 6.1.2.4.6 USB 3.2 Signal Swing

An active cable transmitter only must drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for USB 3.2 Gen2, if the transmitter is located in the cable plug next to the receiving port.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for USB 3.2 Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason. Figure 6-2 defines the SuperSpeed electrical test points and is copied from the **USB 3.2** specification. Figure 6-3 indicates the test points and test equipment connections.

Active cables which include at least one retimer shall meet the requirements in Sections 6.1.2.4.6.1 and 6.1.2.4.6.4. Linear re-driven active cables (LRDs) shall meet the requirements in Table 6-15.

# USB Type-C ENGINEERING CHANGE NOTICE

## d). 6.1.2.5.3 Re-timer-based Active Cable Electrical Requirements, Page 287

### From Text:

#### 6.1.2.5.3 Re-timer-based Active Cable Electrical Requirements

This section describes the electrical requirements and compliance testing for **USB4** re-timer-based active cables.

##### 6.1.2.5.3.1 Output Equalization

A **USB4** active cable *shall* implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization *shall* support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the **USB4** specification, and *shall* be measured at TP3'.

##### 6.1.2.5.3.2 Re-timer-based Active Cable Compliance Test Setup

##### 6.1.2.5.3.3 Cable Compliance Testing

Table 6-13 defines the **USB4** Active Cable specifications for Gen2 and Gen3 systems at TP3'. These parameters *shall* be measured at the Active Cable's output while applying a stressed signal at the input as specified in Table 6-14.

A **USB4** active cable *shall* be tested by injecting several different periodic jitter components, one at a time. The test *shall* include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal *shall* include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to -5300ppm. PRBS31 pattern shall be used for **USB4** active cable compliance testing. However, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise *shall* be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise *shall* be 100 mV peak-to-peak at TP2, where the added noise profile *shall* be sinewave at frequency not smaller than 400 MHz. All the specified jitter values *shall* be calibrated while applying the reference CDR defined in the **USB4** specification.

A **USB4** active cable receiver *may* configure its Link Partner's TX equalizer during the Link establishment. The pattern generator *shall* support tunable 3-tap FIR at its output, which *may* be adjusted during the test by the receiver under test through out-of-band software channel.

#### Table 6-13 Re-timer-based USB4 Active Cable Output Specifications Applied for All Speeds (at TP3')

#### Table 6-14 Stressed Receiver Conditions for USB4 Gen2 and Gen3 Cable Compliance Testing (at TP2)

##### 6.1.2.5.3.4 Cable Error-Bursts Testing

To facilitate proper FEC operation, an active cable receiver *shall* take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see **USB4** specification). The cable receiver under test *shall* trigger on bit-errors and *shall* capture error events that follow.

The test setup *shall* be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude *shall* be increased to the point where uncoded BER of 1E-8 is observed. The receiver under test *shall* trigger on bit-error and *shall* capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits *shall* be examined for errors starting from the initial trigger. The probability for burst renewal *shall* be 5E-7 or less (i.e., one error burst restart per 2 million error captures).

The following is an example analysis:

No burst restart: captured\_data[31:0]=0000000000000000000000001111111111

Burst restart: captured\_data[31:0]=000000000000000000000000111001111111

# USB Type-C ENGINEERING CHANGE NOTICE

where ‘1’ represents a bit error and ‘0’ represents a correct bit, as expected from “exclusive or” (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured\_data[0] corresponds to the error event trigger.

*Note: A burst of errors contains 1 or more consecutive bit errors.*

## 6.1.2.5.3.5 Noise Contributed by Integrated Return-Loss (NRL)

This section will be added in a future ECN.

## To Text:

### 6.1.2.5.3 Re-timer-based Active Cable Electrical Requirements

This section describes the electrical requirements and compliance testing for **USB4** re-timer-based active cables.

#### 6.1.2.5.3.1 Re-timer-based Active Cable Compliance Test Setup

#### 6.1.2.5.3.2 USB4 Gen2/3 Re-timer-based Active Cable

##### 6.1.2.5.3.2.1 Output Equalization

A **USB4 Gen2/3** active cable *shall* implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization *shall* support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the **USB4** specification, and *shall* be measured at TP3’.

##### 6.1.2.5.3.2.2 Cable Compliance Testing

Table 6-13 defines the **USB4 Gen2/3** Active Cable specifications for Gen2 and Gen3 systems at TP3’. These parameters *shall* be measured at the Active Cable’s output while applying a stressed signal at the input as specified in

Table 6-14.

A **USB4 Gen2/3** active cable *shall* be tested by injecting several different periodic jitter components, one at a time. The test *shall* include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal *shall* include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to –5300ppm. PRBS31 pattern shall be used for **USB4 Gen2/3** active cable compliance testing.

However,

calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise *shall* be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise *shall* be 100 mV peak-to-peak at TP2, where the added noise profile *shall* be sinewave at frequency not smaller than 400 MHz. All the specified jitter values *shall* be calibrated while applying the reference CDR defined in the **USB4 Gen2/3** specification.

A **USB4** active cable receiver *may* configure its Link Partner’s TX equalizer during the Link establishment. The pattern generator *shall* support tunable 3-tap FIR at its output, which *may* be adjusted during the test by the receiver under test through out-of-band software channel.

**Table 6-13 Re-timer-based USB4 Gen2/3 Active Cable Output Specifications Applied for All Speeds (at TP3’)**

**Table 6-14 Stressed Receiver Conditions for USB4 Gen2 and Gen3 Cable Compliance Testing (at TP2)**

#### 6.1.2.5.3.4 Cable Error-Bursts Testing

To facilitate proper FEC operation, an active cable ~~receiver~~ *shall* take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see **USB4** specification). The probability of Error-Burst Restart Events should not exceed 5E-7 (less than one restart event per 2 million bursts on average). The combination of an uncoded BER of 1E-12 and an Error-Burst Restart probability of 5E-7 supports an uncoded BER

# USB Type-C ENGINEERING CHANGE NOTICE

of 1E-19. In cases where the actual uncoded BER is less than 1E-21 at a certain ratio, the Error Burst Restart probability can be larger than 5E-7 at the same ratio, since the coded BER depends on the product of the two terms. It is recommended that the cable multi error-bursts probability be characterized using the compliance post processing tool (Informative).

The cable receiver under test ~~shall~~ trigger on bit errors and ~~shall~~ capture error events that follow:

The test setup ~~shall~~ be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward error correction nor pre-coding are applied. After initialization, the periodic jitter magnitude ~~shall~~ be increased to the point where uncoded BER of 1E-8 is observed. The receiver under test ~~shall~~ trigger on bit error and ~~shall~~ capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits ~~shall~~ be examined for errors starting from the initial trigger. The probability for burst renewal ~~shall~~ be 5E-7 or less (i.e., one error burst restart per 2 million error captures).

The following is an example analysis:

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where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive-or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured\_data[0] corresponds to the error event trigger.

Note: A burst of errors contains 1 or more consecutive bit errors.

## 6.1.2.5.3.5 Noise Contributed by Integrated Return Loss (NRL)

This section will be added in a future ECN.

## Added Text: (Tsion to add)

### 6.1.2.5.3.3 USB4 Gen4 Re-timer-based Active Cable

TBD

# USB Type-C ENGINEERING CHANGE NOTICE

## e). 6.1.2.5.4 LRD-based Active Cable Electrical Requirements, Page 291

### From Text:

#### 6.1.2.5.4 LRD-based Active Cable Electrical Requirements

Linear re-driver-based (LRD-based) active cables **shall** be tested as a complete component for compliance. An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).

As shown in Figure 6-9, a compliant USB Type-C receptacle **shall** be connected to both ends of the active cable for injecting and measuring the signal to the corresponding TP2 and TP3 reference points. Details of the Compliance Receptacle and boards can be found in Section 3.3.6 of **USB4** Specification.

#### 6.1.2.5.4.1 General Implementation Notes

This specification was developed considering electrical interoperability with legacy systems, as the LRD-based Active Cables were added to the USB ecosystem in a late phase when a lot of devices were already in the field.

The USB Type-C interconnect ecosystem assumes the worst case 1 m/2 m/0.8 m passive cable is the worst-case connection (for **USB 3.2**, **USB4** Gen2 and **USB4** Gen3 respectively).

The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worst-case passive cable is defined in the **USB 3.2** and **USB4** Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that **shall** meet this requirement.

The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified **USB 3.2** and **USB4** devices is maintained.

For the Gen4 update to the **USB4** specification, LRD-based cable technology was considered, and all TX/RX implications are implicitly comprehended in the base specification.

Given this background, the following are assumptions regarding the LRD-based active cable implementation:

1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).
2. For **USB 3.2** Gen2 and **USB4** Gen2/3, LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the TxFFE training from the receiver.
3. For **USB4** Gen4, it is a valid implementation choice to include AGC in the cable, however the time which this AGC can be enabled is limited to tLRDSelfTune which defined in this specification in Section 6.1.2.5.4.13.
4. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.
5. Receiver systems rely on the low-pass-filter nature of the cable and having an over-equalized cable (i.e., weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the cable **should** be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.
6. During the development of the **USB4** Gen4 LRD cable we used a set of design assumptions that can be found in Appendix J.
- 7.

### To Text:

#### 6.1.2.5.4 LRD-based Active Cable Electrical Requirements

Linear re-driver-based (LRD-based) active cables **shall** be tested as a complete component for compliance. An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).



# USB Type-C ENGINEERING CHANGE NOTICE

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The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worst-case passive cable is defined in the **USB 3.2** and **USB4** Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that **shall** meet this requirement.

The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified **USB 3.2** and **USB4** devices is maintained.

For the Gen4 update to the **USB4** specification, LRD-based cable technology was considered, and all TX/RX implications are implicitly comprehended in the base specification.

Given this background, the following are assumptions regarding the LRD-based active cable implementation:

1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).
2. For **USB 3.2** Gen2 and **USB4** ~~Gen2/3~~, LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the TxFFE training from the receiver.
3. For **USB4** Gen4, it is a valid implementation choice to include AGC in the cable, however the time which this AGC can be enabled is limited to tLRDSelfTune which defined in this specification in Section 6.1.2.5.4.13.
4. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.
5. Receiver systems rely on the low-pass-filter nature of the cable and having an over-equalized cable (i.e., weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the cable **should** be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.
6. During the development of the **USB4** Gen4 LRD cable we used a set of design assumptions that can be found in Appendix J.

# USB Type-C ENGINEERING CHANGE NOTICE

## f). 6.1.2.5.4.14 USB4 Gen4 Lane Direction Change, Page 298

### From Text:

#### 6.1.2.5.4.14 **USB4** Gen4 Lane Direction Change

LRD-based active cables that support **USB4** Gen4 **shall** support the asymmetric mode as defined in the **USB4** specification (Section 4.2.2.5) and the LRD\_Tuning.Force\_Lane\_Reversal for cable compliance. That means that each high-speed pair of the cable (TX0/TX1/RX0/RX1) **shall** be able to operate in both directions. The cable **shall** follow 6.1.2.5.4.16.5 and 6.1.2.5.4.16.6 when switching into and out of asymmetric mode.

### To Text:

#### 6.1.2.5.4.14 **USB4** Gen4 Lane Direction Change

LRD-based active cables that support **USB4** Gen4 **shall** support the asymmetric mode as defined in the **USB4** specification (Section 4.2.2.5) ~~and the LRD\_Tuning.Force\_Lane\_Reversal~~ for cable compliance. That means that each high-speed pair of the cable (TX0/TX1/RX0/RX1) **shall** be able to operate in both directions. The cable **shall** follow 6.1.2.5.4.16.5 and 6.1.2.5.4.16.6 when switching into and out of asymmetric mode.

# USB Type-C ENGINEERING CHANGE NOTICE

## g). Table 6-19 USB4 Gen4 Active Cable SBx Transaction Snooping, Page 300

### From Text:

Table 6-19 USB4 Gen4 Active Cable SBx Transaction Snooping

Transaction Type	Symbol or Transaction Contents	Optional or Required?	Action
LT	LT_Fall	Required	Transition to CLd.
	LT_Resume	<b>Optional</b> if LOS (loss of signal) is used	Transition to Forwarding.
	LT_LROff	Required	Transition to CLd. Issued on Lane 0 but affects all both lanes.
	LT_SwitchRx2Tx	Required	Transition to/from Asymmetrical when snooped on SBU1.
	LT_SwitchAck	Required	Transition to/from Asymmetrical when snooped on SBU1.
	LT_Gen2	<b>Optional</b> if LOS is used	Transition to Forwarding. <b>Optional</b> to use specific Gen2 fixed gain and equalization.
	LT_Gen3	<b>Optional</b> if LOS is used	Transition to Forwarding. <b>Optional</b> to use specific Gen3 fixed gain and equalization.
	LT_Fall	Required	Transition to CLd.
RT Broadcast	<b>TBT3-CompatibleSpeed</b>	<b>Optional</b>	Modify gain and equalization for TBT rates.
	<b>USB4</b>	Required	0b – Use LT transactions for link training. 1b – Use RT transactions for link training.
	SelectedGen	<b>Optional</b>	Modify gain and equalization per data rate Gen2, Gen3, Gen4.
	Enable3Tx	Required	Asymmetrical Initial link training.
	Enable3Rx	Required	Asymmetrical Initial link training.
	Lane1Enabled	<b>Optional</b> if LOS is used	0b – CLd lane1. 1b – Enable forwarding lane1.
	Lane0Enabled	<b>Optional</b> if LOS is used	0b – CLd lane0. 1b – Enable forwarding lane0.
RT Addressed Index 0 to Gen4TxFFE	Partner_Tx_Status_Byte.TxFFE_Start	<b>Optional</b>	Adjustment of AGC is allowed.
	Partner_Tx_Status_Byte.Request_Done	<b>Optional</b>	0b – Do not start AGC. 1b – start AGC for tLRDSelfTune.
RT Addressed Index 0 to LRD Tuning	Force Lane Reversal (bit 1)	Required	Required for Compliance Force Lane Reversal. <b>Optional</b> to adjust gain and equalization in a TBD way.
ELT	ELT_OpDone	<b>Optional</b>	No action.
	ELT_Recovery	Required	Transition to Forwarding.

# USB Type-C ENGINEERING CHANGE NOTICE

## 6.1.2.5.4.16 USB4 and TBT3 Logical Layer

The LRD active cable **shall** determine its **USB4** behavior based on snooping the RT broadcast (RTb) and RT addressed (RTa) transactions, the LT, and the ELT transactions.

## To Text:

## 6.1.2.5.4.16 USB4 and TBT3 Logical Layer

The LRD active cable **shall** determine its **USB4** behavior based on snooping the LT, ELT, RT broadcast (RTb) and RT addressed (RTa) transactions, ~~the LT, and the ELT transactions.~~

Table 6-19 **USB4 Gen4** Active Cable SBx Transaction Snooping

Transaction Type	Symbol or Transaction Contents	Optional or Required?	USB4/TBT Generation	Action
LT	LT_Fall	Required	TBT3	Transition to CLd.
	LT_Resume	<b>Optional</b> if LOS (loss of signal) is used	TBT3	Transition to Forwarding.
	LT_LROff	Required	All	Transition to CLd. Issued on Lane 0 but affects all both lanes.
	LT_SwitchRx2Tx	Required	Gen4	Transition to/from Asymmetrical when snooped on SBU1.
	LT_SwitchAck	Required	Gen4	Transition to/from Asymmetrical when snooped on SBU1.
	LT_Gen2	<b>Optional</b> if LOS is used	TBT3	Transition to Forwarding. <b>Optional</b> to use specific Gen2 fixed gain and equalization.
	LT_Gen3	<b>Optional</b> if LOS is used	TBT3	Transition to Forwarding. <b>Optional</b> to use specific Gen3 fixed gain and equalization.
	<del>LT_Fall</del>	<del>Required</del>		<del>Transition to CLd.</del>
RT Broadcast	<del>TBT3-CompatibleSpeed</del>	<del>Optional</del>	TBT3	Modify gain and equalization for TBT rates.
	<b>USB4</b>	Required	All	0b – Use LT transactions for link training. 1b – Use RT transactions for link training.
	SelectedGen	<b>Optional</b>	All	Modify gain and equalization per data rate Gen2, Gen3, Gen4.
	Enable3Tx	Required	Gen4	Asymmetrical Initial link training.
	Enable3Rx	Required	Gen4	Asymmetrical Initial link training.

# USB Type-C ENGINEERING CHANGE NOTICE

Transaction Type	Symbol or Transaction Contents	Optional or Required?	USB4/TBT Generation	Action
	Lane1Enabled	<i>Optional</i> if LOS is used	All	0b – CLd lane1. 1b – Enable forwarding lane1.
	Lane0Enabled	<i>Optional</i> if LOS is used	All	0b – CLd lane0. 1b – Enable forwarding lane0.
RT Addressed Index 0 to Gen4TxFFE	Partner_Tx_Status_Byte.TxFFE_Start	<i>Optional</i>	Gen4	Adjustment of AGC is allowed.
	Partner_Tx_Status_Byte.Request_Done	<i>Optional</i>	Gen4	0b – Do not start AGC. 1b – start AGC for tLRDSelfTune.
<del>RT Addressed Index 0 to LRD Tuning</del>	<del>Force Lane Reversal (bit 1)</del>	<del>Required</del>	Gen4	<del>Required for Compliance Force Lane Reversal. <i>Optional</i> to adjust gain and equalization in a TBD way.</del>
ELT	ELT_OpDone	<i>Optional</i>	Gen4	No action.
	ELT_Recovery	Required	Gen4	Transition to Forwarding on both lanes

# USB Type-C ENGINEERING CHANGE NOTICE

## h). 6.1.2.5.4.16.3 *USB4* and *TBT3* Lane Initialization. *USB4* Requirements, Page 302

### From Text:

#### *USB4* Requirements:

1. Snooped Broadcast RT transactions on SBU1:
  - a. ***USB4***: If the ***USB4*** bit is set to 1b, addressed RT transactions are used for link training.
  - b. SelectGen: Set fixed gain and equalization. It is ***optional*** for the gain and equalization to change based on the speed indication.
  - c. Lane0Enabled, Lane1Enabled: Enable forwarding if Enable3Tx or Enable3Rx are not enabled. The LRD ***shall*** enable forwarding in tLRDForward after snooping the Lane Enable. ***Optional*** to use LOS to enable forwarding.
  - d. Enable3Tx: Enable three transmitters and one receiver as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
  - e. Enable3Rx: Enable three receivers and one transmitter as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
2. Snooped Addressed RT transaction to SB Register Gen\_4\_TxFFE with Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE:
  - a. If Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE (bit 7) =1b, the LRD ***may*** adjust its AGC in Phase 5.
  - b. If Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE (bit 7) =0b, the LRD ***may not*** adjust its AGC in Phase 5.
  - c. Note that the bytes in Gen4TxFFE.Tx\_Status\_Byte change if the link is initialized as an asymmetrical link. Refer to the ***USB4*** V2 specification for details.
3. Snooped addressed RT transaction to SB Register LRD\_Tuning on SBU1:
  - a. If LRD\_Tuning.Force\_Lane\_Reversal=0b, use normal Lane1 and Lane2 operation relative to CC without changing the SBU1/2.
  - b. If LRD\_Tuning.Force\_Lane\_Reversal=1b, swap Lane1 and Lane2 without changing the SBU1/2. The lane reversal ***shall*** complete within tLRDSelfTune.

### Phase 5: Link Equalization

#### Requirements (only applies to ***USB4*** Gen4):

1. Snooped addressed RT transaction to SB Register Gen\_4\_TxFFE:
  - a. Partner\_Tx\_Status\_Byte.Request\_Done (bit 6)=1b is the indication to the LRD to start the AGC training in the SBU1 to SBU2 direction.
  - b. The LRD active cable AGC ***shall*** complete its adjustments within tLRDSelfTune. If there are two LRDs in the cable, each ***may*** be adjusted independently but tLRDSelfTune ***shall*** be met for the cable assembly.
2. Snooped addressed RT transaction to SB Register LRD\_Tuning on SBU1:
  - a. ***Optionally*** save the entire LRD\_Tuning register. The LRD ***may optionally*** adjust its gain in a TBD way based on the contents of the register. The LRD ***shall*** complete its gain

# USB Type-C ENGINEERING CHANGE NOTICE

adjustment in tLRDSelfTune minimum time (**USB4** V2 specification) when it snoops a write to LRD\_Tuning.

An example of link training with LRD AGC adjustment is indicated in Figure 6-13.

Note: The LRD has no sideband indication of the switch from PAM2 to PAM3 and AGC training must function on both PAM2 and PAM3 incoming data.

## To Text:

### USB4 Requirements:

4. Snooped Broadcast RT transactions on SBU1:
  - a. **USB4**: If the **USB4** bit is set to 1b, addressed RT transactions are used for link training.
  - b. SelectGen: Set fixed gain and equalization. It is **optional** for the gain and equalization to change based on the speed indication.
  - c. Lane0Enabled, Lane1Enabled: Enable forwarding if Enable3Tx or Enable3Rx are not enabled. The LRD **shall** enable forwarding in tLRDForward after snooping the Lane Enable. **Optional** to use LOS to enable forwarding.
  - d. Enable3Tx: Enable three transmitters and one receiver as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
  - e. Enable3Rx: Enable three receivers and one transmitter as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
5. Snooped Addressed RT transaction to SB Register Gen\_4\_TxFFE with Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE:
  - a. If Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE (bit 7) =1b, the LRD **may** adjust its AGC in Phase 5.
  - b. If Gen4TxFFE.Tx\_Status\_Byte.Start\_TXFFE (bit 7) =0b, the LRD **may not** adjust its AGC in Phase 5.
  - c. Note that the bytes in Gen4TxFFE.Tx\_Status\_Byte change if the link is initialized as an asymmetrical link. Refer to the **USB4** V2 specification for details.

### ~~6. Snooped addressed RT transaction to SB Register LRD\_Tuning on SBU1:~~

- ~~a. If LRD\_Tuning.Force\_Lane\_Reversal=0b, use normal Lane1 and Lane2 operation relative to CC without changing the SBU1/2.~~
- ~~b. If LRD\_Tuning.Force\_Lane\_Reversal=1b, swap Lane1 and Lane2 without changing the SBU1/2. The lane reversal **shall** complete within tLRDSelfTune.~~

## Phase 5: Link Equalization

### Requirements (only applies to **USB4** Gen4):

3. Snooped addressed RT transaction to SB Register Gen\_4\_TxFFE:
  - a. Partner\_Tx\_Status\_Byte.Request\_Done (bit 6)=1b is the indication to the LRD to start the AGC training in the SBU1 to SBU2 direction.

# USB Type-C ENGINEERING CHANGE NOTICE

- b. The LRD active cable AGC **shall** complete its adjustments within tLRDSelfTune. If there are two LRDs in the cable, each **may** be adjusted independently but tLRDSelfTune **shall** be met for the cable assembly.

## ~~4. Snooped-addressed RT transaction to SB Register LRD\_Tuning on SBU1:~~

- a. ~~**Optionally** save the entire LRD\_Tuning register. The LRD **may optionally** adjust its gain in a TBD way based on the contents of the register. The LRD **shall** complete its gain adjustment in tLRDSelfTune minimum time (**USB4** V2 specification) when it snoops a write to LRD\_Tuning.~~

An example of link training with LRD AGC adjustment is indicated in Figure 6-13.

Note: The LRD has no sideband indication of the switch from PAM2 to PAM3 and AGC training must function on both PAM2 and PAM3 incoming data.



# USB Type-C ENGINEERING CHANGE NOTICE

## i). 6.1.2.5.4.16.4.2 Forwarding, Page 305

### From Text:

#### 6.1.2.5.4.16.4.2 Forwarding

##### Entry to State

The LRD **shall** enter this state on the following events:

- Any SBU1 (or **optionally** SBU2) transaction which is not LT\_Fall or LT\_Lroff
- After exiting Low Power state
- Snooping ELT\_Recovery

##### Behavior in State

- Enable the LOS receiver.
- Snoop SBU1 (and **optionally** SBU2).
- Determine the direction of the lanes if **USB4** Gen4.
- Ramp the common mode voltage if needed as defined in the link training.
- Forward the high-speed data. Use the last known AGC setting if the transition was from Low Power or ELT\_Recovery.
- Forward the high-speed data and adjust the AGC per Phase 4 and 5 Link training if Gen4.
- Forward the high-speed data and use the fixed stored AGC and EQ if Gen2 or Gen3.

##### Exit from State

- Transition to CLd on detection of low on SBU1 (or **optionally** SBU2) for greater than tDisconnectRx or upon snooping LT\_Fall or LT\_Lroff.
- Transition to Low Power if LOS is detected per lane.

### To Text:

#### 6.1.2.5.4.16.4.2 Forwarding

##### Entry to State

The LRD **shall** enter this state on the following events:

- Any SBU1 (or **optionally** SBU2) transaction which is not LT\_Fall or LT\_Lroff
- After exiting Low Power state
- Snooping ELT\_Recovery

##### Behavior in State

- Enable the LOS receiver.
- Snoop SBU1 (and **optionally** SBU2).
- Determine the direction of the lanes if **USB4** Gen4.

# USB Type-C ENGINEERING CHANGE NOTICE

- Ramp the common mode voltage if needed as defined in the link training.
- Forward the high-speed data. Use the last known AGC setting if the transition was from Low Power or ELT\_Recovery.
- Forward the high-speed data and adjust the AGC per Phase 4 and 5 Link training if Gen4.
- Forward the high-speed data and use the fixed stored AGC ~~and EQ~~ if Gen2 or Gen3.
- If Entry to Forwarding was from ELT\_Recovery, both lanes shall enable forwarding.

## Exit from State

- Transition to CLd on detection of low on SBU1 (or *optionally* SBU2) for greater than tDisconnectRx or upon snooping LT\_Fall or LT\_Lroff.
- Transition to Low Power if LOS is detected per lane.

# USB Type-C ENGINEERING CHANGE NOTICE

## j). 6.1.2.5.4.16.4.3 Low Power State, Page 305

### From Text:

#### 6.1.2.5.4.16.4.3 Low Power State

The low power state is used to conserve power in electrical idle.

#### Entry to State

- USB4 gen2/3 and TBT3/4: Transition to Low Power when detecting no high-speed signal on the Rx input per lane.
- USB4 gen3: Transition to Low Power when detecting no high-speed signal on a channel.

#### Behavior in State

- Snoop SBU1 (and *optionally* SBU2).
- Common mode voltage **shall** be maintained.
- Terminations **shall** be maintained.
- Consume less power than in Forwarding.

#### Exit from State

- Transition to Forwarding:
  - USB4 gen2/3 and TBT3/4: Detection of LFPS on any channel **shall** transition the LRD to Forwarding on the channel receiving the LFPS and the channel on the same lane in the opposite direction. Note that LFPS **may** be on only one channel (one lane in one direction) if the link is in CL0s.
  - USB4 gen4: Detection of LFPS on any channel **shall** transition the LRD to Forwarding on both channels in both directions.
  - The LRD active cable **shall** consume a maximum of eight LFPS when transitioning to Forwarding.
  - The LRD **shall not** forward LFPS until it has enabled forwarding in both directions. Refer to Figure 6-15.
  - Snoop of ELT\_Recovery

Note: The LRD shall meet the electrical requirements when forwarding LFPS

- Transition to CLd:
  - If SBU1 (or *optionally* SBU2) is low for greater than tDisconnectRx or if LT\_Fall, or LT\_LR\_Off is detected.
  - The transmitter and receiver **shall** maintain the common-mode voltage and terminations.

# USB Type-C ENGINEERING CHANGE NOTICE

## To Text:

### 6.1.2.5.4.16.4.3 Low Power State

The low power state is used to conserve power in electrical idle.

#### Entry to State

- USB4 gen2/3 and TBT3/4: Transition to Low Power when detecting no high-speed signal on the Rx input per lane.
- USB4 gen~~3~~4: Transition to Low Power when detecting no high-speed signal on a channel.

#### Behavior in State

- Snoop SBU1 (and *optionally* SBU2).
- Common mode voltage *shall* be maintained.
- Terminations *shall* be maintained.
- Consume less power than in Forwarding.

#### Exit from State

- Transition to Forwarding:
  - USB4 gen2/3 and TBT3/4: Detection of LFPS on any channel *shall* transition the LRD to Forwarding on the channel receiving the LFPS and the channel on the same lane in the opposite direction. Note that LFPS *may* be on only one channel (one lane in one direction) if the link is in CL0s.
  - USB4 gen4: Detection of LFPS on any channel *shall* transition the LRD to Forwarding on both channels in both directions.
  - The LRD active cable *shall* consume a maximum of eight LFPS when transitioning to Forwarding.
  - The LRD *shall not* forward LFPS until it has enabled forwarding in both directions. Refer to Figure 6-15.
  - Snoop of ELT\_Recovery

Note: The LRD shall meet the electrical requirements when forwarding LFPS

- Transition to CLd:
  - If SBU1 (or *optionally* SBU2) is low for greater than tDisconnectRx or if LT\_Fall, or LT\_LR\_Off is detected.

The transmitter and receiver *shall* maintain the common-mode voltage and terminations.

# USB Type-C ENGINEERING CHANGE NOTICE

## k). 6.1.2.5.4.17 Cable Compliance, Page 310

### From Text:

#### 6.1.2.5.4.17 Cable Compliance

The LRD in the active cable **shall** support snooping the LRD Tuning register as defined in Table 6-21. The Compliance Software only writes to the LRD Tuning Register if it needs to swap Lane1 and Lane2 in the active cable. The Compliance Software first writes to the Router LRD Tuning Register to set Force Lane Reversal=1b with Response Request=1b. The connected Router will then write to the LRD Tuning register in the test equipment with the same Force Lane Reversal=1b with Response Request=0. This allows LRD active cables which only snoop SBU1 to snoop the LRD Tuning Register write on the cable plug farthest from the Compliance Software and test equipment.

The Compliance Software then writes to the LRD Tuning register to set Force Lane Reversal=1b with Response Request=0b to inform the local cable plug.

The active cable **shall** switch back to normal Lane1 and Lane2 operation on disconnect.

**Table 6-21 USB4 LRD Tuning Register Snooping**

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
7	LRD Tuning	0	0	<b>Response Request</b> – When this bit is set to 1b, the <b>USB4</b> Port <b>shall</b> send a write Command to the LRD Tuning register in the adjacent Router/Re-timer. The write <b>shall</b> contain the values of the local LRD Tuning register and <b>shall</b> have the Response Request bit set to 0b. The <b>USB4</b> Port <b>shall</b> then set this bit to 0b.	R	0
			1	<b>Force Lane Reversal</b> – Identifies whether to override the functional Lane Reversal.  0b: Cable <b>shall</b> use normal Lane1 and Lane2 operation relative to CC  1b: Cable <b>shall</b> swap Lane1 and Lane2  Note: Sideband SBU1 and SBU2 <b>shall</b> remain in normal orientation regardless of the Force Lane Reversal setting.	R	0

### To Text:

#### ~~6.1.2.5.4.17 Cable Compliance~~

~~The LRD in the active cable **shall** support snooping the LRD Tuning register as defined in Table 6-21. The Compliance Software only writes to the LRD Tuning Register if it needs to swap Lane1 and Lane2 in the active cable. The Compliance Software first writes to the Router LRD Tuning Register to set Force Lane Reversal=1b with Response Request=1b. The connected Router will then write to the LRD Tuning register in the test equipment with the same Force Lane Reversal=1b with Response Request=0. This allows LRD active cables which only snoop SBU1 to snoop the LRD Tuning Register write on the cable plug farthest from the Compliance Software and test equipment.~~

~~The Compliance Software then writes to the LRD Tuning register to set Force Lane Reversal=1b with Response Request=0b to inform the local cable plug.~~

# USB Type-C ENGINEERING CHANGE NOTICE

The active cable **shall** switch back to normal Lane1 and Lane2 operation on disconnect.

**Table 6-21 ~~USB4~~ LRD Tuning Register Snooping**

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
7	LRD Tuning	0	0	<del>Response Request</del> —When this bit is set to 1b, the <del>USB4</del> Port <b>shall</b> send a write Command to the LRD Tuning register in the adjacent Router/Re-timer. The write <b>shall</b> contain the values of the local LRD Tuning register and <b>shall</b> have the Response Request bit set to 0b. The <del>USB4</del> Port <b>shall</b> then set this bit to 0b.	R	0
			1	<del>Force Lane Reversal</del> —Identifies whether to override the functional Lane Reversal.  0b:—Cable <b>shall</b> use normal Lane1 and Lane2 operation relative to CC  1b:—Cable <b>shall</b> swap Lane1 and Lane2  Note: Sideband SBU1 and SBU2 <b>shall</b> remain in normal orientation regardless of the Force Lane Reversal setting.	R	0